

TSMC-01-846B

February 9, 2004

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject:

Serial No. 10/726,104 12/02/03

Chi-Wen Liu et al.

A COMPLETELY ENCLOSED COPPER
STRUCTURE TO AVOID COPPER DAMAGE
FOR DAMASCENE PROCESSES

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation
In An Application.

The following Patents and/or Publications are submitted to
comply with the duty of disclosure under CFR 1.97-1.99 and
37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being
deposited with the United States Postal Service as first class
mail in an envelope addressed to: Commissioner for Patents,
P.O. Box 1450, Alexandria, VA 22313-1450 on February 17, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

Stephen B. Ackerman 2/17/04

The following two U.S. Patents describe a multilevel metallization process using polishing:

- 1) U.S. Patent 5,380,546 to Krishnan et al., "Multilevel Metallization Process for Electronic Components."
- 2) U.S. Patent 5,451,551 to Krishnan et al., "Multilevel Metallization Process Using Polishing."

U.S. Patent 6,251,786 to Zhou et al., "Method to Create a Copper Dual Damascene Structure with Less Dishing and Erosion," describes a dual damascene interconnect with a silicon nitride (Si_3N_4) film 34 over the recessed dual damascene interconnect.

U.S. Patent 6,258,713 to Yu et al., "Method for Forming Dual Damascene Structure," describes a dual damascene interconnect with a TiN layer over the planarized dual damascene interconnect.

U.S. Patent 6,274,499 to Gupta et al., "Method to Avoid Copper Contamination During Copper Etching and CMP," describes a dual damascene process with a dielectric cap 30.

The article entitled "Finding the Ultimate Copper Barrier and Seed," Peters; Semiconductor International; July 2001; page 23, describes various barrier/liner materials such as WN, TaN, TaN + Co, TiN and TiN + PVD Cu.



SMC-01-846B

The following three U.S. Patents describe barrier/CMP stop layers over damascene structures:

- 1) U.S. Patent 6,114,246 to Weling, "Method of Using a Polish Stop Film to Control Dishing During Copper Chemical Mechanical Polishing."
- 2) U.S. Patent 6,103,625 to Marcyk et al., "Use of a Polish Stop Layer in the Formation of Metal Structures."
- 3) U.S. Patent 6,083,835 to Shue et al., "Self-Passivation of Copper Damascene."

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761



Form PTO-1449	DocId Number (Optional) TSMC-01-846B	Application Number 10/726,104
INFORMATION DISCLOSURE CITATION IN AN APPLICATION <small>(Use several sheets if necessary)</small>	Applicant Chi-Wen Liu et al.	
	Filing Date 12/02/03	Group Art Unit

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILED DATE IF APPROPRIATE
	5380546	11/10/95	Krishnan et al.	427	126.1	6/9/93
	5451551	9/19/95	Krishnan et al.	437	241	8/15/94
	6251786	6/26/01	Zhou et al.	438	692	9/7/99
	6258713	7/10/01	Yu et al.	438	634	12/3/99
	6274499	8/14/01	Gupta et al.	438	692	11/19/99
	6114246	9/5/00	Weling	438	691	1/7/99
	6103625	8/15/00	Marcynk et al.	438	691	12/31/97
	6083835	7/4/00	Shue et al.	438	687	7/24/98

FOREIGN PATENT DOCUMENTS

DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
					YES	NO

OTHER DOCUMENTS (Including Author, Title, Date, Portion of Pages, Etc.)

-	The article entitled "Finding the Ultimate Copper Barrier and Seed" by Peters, Semiconductor International, July 2001, p. 23.

EXAMINER	DATE CONSIDERED
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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.